PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPG-PWR/14/8552
Dated 23 Jun 2014

DPAK Matrix Large Die Pad Back-End Capacity Extension -

Nantong Fujitsu Microelectronics (China)

Table 1. Change Implementation Schedule

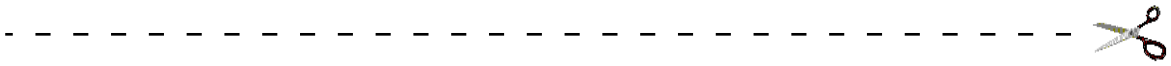
Forecasted implementation date for change	16-Jun-2014
Forecasted availability date of samples for customer	16-Jun-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	16-Jun-2014
Estimated date of changed product first shipment	22-Sep-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Package assembly process change
Reason for change	Improve service to Customers
Description of the change	Continuing in the aim of a constant process improvement, please be informed that we're going to use Automatic Assembly/Testing DPAK Matrix & Large Die Pad line for Selected Power BIPOLAR and Power MOSFET Transistors produced in Nantong Fujitsu Microelectronics (China). You may already receive products in DPAK Matrix & Large Die Pad line from Longgang or Shenzhen (China). DPAK device products, manufactured in Nantong Fujitsu Microelectronics (China), guarantee the same quality and electrical characteristics as reported in the relevant data sheets. Devices used for qualification are available as samples.
Change Product Identification	by data code.
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPG-PWR/14/8552**
Please sign and return to STMicroelectronics Sales Office	**Dated 23 Jun 2014**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Mottese, Anna	Marketing Manager
Aleo, Mario-Antonio	Product Manager
Falcone, Giuseppe	Q.A. Manager

Dear Customer,

Continuing in the aim of a constant process improvement, please be informed that we're going to use Automatic Assembly/Testing DPAK Matrix & Large Die Pad line for Selected Power BIPOLAR and Power MOSFET Transistors produced in Nantong Fujitsu Microelectronics (China). You may already receive products in DPAK Matrix & Large Die Pad line from Longgang or Shenzhen (China). DPAK device products, manufactured in Nantong Fujitsu Microelectronics (China), guarantee the same quality and electrical characteristics as reported in the relevant data sheets. Devices used for qualification are available as samples.

The involved product series and affected packages are listed in the attached file.

Any other Product related to the above series, manufactured in Nantong Fujitsu Microelectronics (China), even if not expressly included or partially mentioned in the attached table, is affected by this change.

Qualification program and results availability:

The reliability test report is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 23-2014.
Any other sample request will be processed and scheduled by Power Transistor Division upon request.

Product Family Description	Package	Part Number - Test Vehicle
Power MOSFET Transistors Power BIPOLAR Transistors	DPAK	STD5NK60ZT4 BUL742C

Change implementation schedule:

The production start and first shipments will be implemented according to our work in progress and materials availability:

Product Family	1st Shipments
Power MOSFET Transistors Power BIPOLAR Transistors	From Week 36-2014

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 days period will constitute acceptance of the change (Jedec Standard No. 46-C). In any case, first shipment may start earlier with customer written agreement.

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of Power BIPOLAR and Power MOSFET Transistors produced in Nantong Fujitsu Microelectronics (China) will be ensured by the Q.A. number marked on the package.

Sincerely Yours.

Reliability Report

DPAK Matrix Large Die Pad Back-End Capacity Extension - Nantong Fujitsu Microelectronics (China)

General Information	
Product Lines:	EZ63 – IV61
Product Families:	Power MOSFET (EZ63) Power BIPOLAR (IV61)
P/Ns:	STD5NK60ZT4 (EZ63) BULD742CT4 (IV61)
Product Group:	IPG
Product division:	Power Transistor Division
Package:	DPAK
Silicon Process techn.:	Zener-Protected SuperMESH™ MOSFET Power BIPOLAR

Locations	
Wafer Diffusion Plants:	Ang Mo Kio (Singapore)
EWS Plants:	Ang Mo Kio (Singapore)
Assembly and testing plant:	*Nantong Fujitsu Microelectronics (NFME) (China)*
Reliability Lab:	*IPG-PTD Catania Reliability Lab.*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	June 2014	8	A. Settinieri	C. Cappello	First issue

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Reliability evaluation for assembly and testing DPAK Matrix Large Die Pad Back-End Capacity Extension - Nantong Fujitsu Microelectronics (China)

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

N-channel Power MOSFET
Power BIPOLAR

4.2 Construction note

D.U.T.: STD5NK60ZT4 LINE: EZ63 PACKAGE: DPAK

Wafer/Die fab. Information	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	Zener-Protected SuperMESH™ MOSFET
Die finishing back side	Ti/Ni/Ag
Die size	3900 x 2890 μm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	Nantong Fujitsu Microelectronics (NFME)
Package description	DPAK
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg Gate – Al Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Nantong Fujitsu Microelectronics (NFME)
Tester	TESEC

D.U.T.: BULD742CT4 LINE: IV61 PACKAGE: DPAK

Wafer/Die fab. Information	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	NPN Power BIPOLAR
Die finishing back side	Ti/Ni/Au
Die size	2430 x 2460 μm^2
Metal	Al/Si
Passivation type	PSG

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	Nantong Fujitsu Microelectronics (NFME)
Package description	DPAK
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg Gate – Al Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Nantong Fujitsu Microelectronics (NFME)
Tester	TESEC

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	STD5NK60ZT4	EZ63	Power MOSFET
2	BULD742CT4	IV61	Power BIPOLAR

5.2 Reliability test plan summary

Lot. 1 - D.U.T.: STD5NK60ZT4 LINE: EZ63 PACKAGE: DPAK

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
						Lot 1
Die Oriented Tests						
HTRB	N	JESD22 A-108	T.A.=150°C Vdss=480V	77	168 H 500 H 1000 H	0/77
HTGB	N	JESD22 A-108	TA = 150°C Vgss= 30V	77	168 H 500 H 1000 H	0/77
HTS	N	JESD22 A-103	TA = 150°C	77	168 H 500 H 1000 H	0/77
Package Oriented Tests						
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times	308	Final	0/308
H3TRB	Y	JESD22 A-101	Ta=85°C Rh=85%, Vdss=100V	77	168 H 500 H 1000 H	0/77
TC	Y	JESD22 A-104	TA=-65°C TO 150°C (1 HOUR/CYCLE)	77	100 cy 200 cy 500 cy	0/77
TF/IOL	Y	Mil-STD 750D Method 1037	ΔTC=105°C	77	5K cy 10K cy	0/77
AC	Y	JESD22 A-102	TA=121°C – PA=2 ATM	77	96 H	0/77

Lot. 2 - D.U.T.: BULD742CT4 LINE: IV61 PACKAGE: DPAK

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS Lot 2
Die Oriented Tests						
HTRB	N	JESD22 A-108	T.A.=150°C Vdss=480V	77	168 H 500 H 1000 H	0/77
HTS	N	JESD22 A-103	TA = 150°C	77	168 H 500 H 1000 H	0/77
Package Oriented Tests						
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times	308	Final	0/308
H3TRB	Y	JESD22 A-101	Ta=85°C Rh=85%, Vdss=100V	77	168 H 500 H 1000 H	0/77
TC	Y	JESD22 A-104	TA=-65°C TO 150°C (1 HOUR/CYCLE)	77	100 cy 200 cy 500 cy	0/77
TF/IOL	Y	Mil-STD 750D Method 1037	ΔTC=105°C	77	5K cy 10K cy	0/77
AC	Y	JESD22 A-102	TA=121°C – PA=2 ATM	77	96 H	0/77

6 ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
Die Oriented Tests		
HTRB High Temperature Reverse Bias **HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented Tests		
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

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